In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims. A complete listing of claims is below with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing:

1. Canceled.

2. (Currently amended) The apparatus as claimed in claim [[1]] 27 further comprising a first delay element coupled to the output of the logic element, the delay element having an output coupled to the reset element of the second storage element and a second delay element with an input coupled to the output of the logic element, the second delay element having an output coupled to the reset element of the first storage element and wherein the delay introduced by the second delay element to the first storage element is less than the delay introduced by the first delay element to the second storage element.

3. (Currently amended) The apparatus as claimed in claim [[1]] 27 further including a first delay element coupled to the output of the logic element, the delay element having an output coupled to the reset element of the second storage element and a second delay element coupled between the logic element and the first delay element, the output of the second delay element being coupled to the reset element of the first storage element and the input of the first delay element.

4. (Currently amended) The apparatus of claim [[1]] 27 wherein the logic element comprises a logic AND gate.

5. (Currently amended) The apparatus of claim [[1]] 27 wherein the two storage elements are flip flops.

6. (Original) The apparatus of claim 5 wherein the flip-flops are D type flip flops and further comprise data inputs coupled to a logic high.

7. (Currently amended) The apparatus of claim [[1]] 27 wherein the output of the first storage element and the output of the second storage element are coupled to a first current source having an enable input coupled to the output of the first storage element and a second current source having an enable input coupled to the output of the second storage element, the first and second current sources being coupled to form an output for [[a]] the phase difference signal.

8. (Currently amended) The apparatus as claimed in claim [[1]] 27 wherein the phase detection apparatus is a tri-state phase frequency detector.

9. (Currently amended) The apparatus as claimed in claim [[1]] 27 wherein the relative delay between the trailing edges of the outputs of the first and second storage elements is programmable.

10. (Previously presented) The apparatus as claimed in claim 9 wherein the relative delay is at least greater than the maximum deviation of the phase of the second storage element's clock input relative to the first storage element's clock input.

11. Canceled

12. (Currently amended) The phase lock loop apparatus as claimed in claim [[11]] 27 wherein the frequency dividing element comprises an interpolator

13. Canceled

14. (Currently amended) The apparatus as claimed in claim [[13]] 27 further comprising:
    a) a delay element coupled to the output of the logic element, the delay element having an output coupled to the reset input of at least one of the first and second storage elements.

15. (Original) The apparatus as claimed in claim 14 wherein the output of the delay element is coupled to the reset element of the first storage element.

16. (Original) The apparatus as claimed in claim 14 wherein the output of the delay element is coupled to the reset element of the second storage element.

17. (Original) The apparatus as claimed in claim 14 wherein the output of the delay element is coupled to the reset element of both the first and second storage elements.

18. (Currently amended) The apparatus as claimed in claim [[13]] 27 wherein the stretching element stretches the trailing edge output of the first storage element relative to the trailing edge output of the second storage element.

19. (Currently amended) The apparatus as claimed in claim [[13]] 27 wherein the stretching element stretches the trailing edge output of the second storage element relative to trailing edge output of the first storage element.

20. (Currently amended) The apparatus as claimed in claim [[13]] 27 wherein the stretching element is located at the output of the first storage element.

21. (Currently amended) The apparatus as claimed in claim [[13]] 27 wherein the stretching element is located at the output of the second storage element.

22. Canceled.

23. (Currently amended) The apparatus as claimed in claim [[13]] 27 wherein [[the]] a delay in the trailing edge is programmable.

24. (Previously presented) The apparatus as claimed in claim 23 wherein the delay is at least greater than the maximum deviation of the phase of the second storage element's clock input relative to the first storage element's clock input.

25. Canceled

26. (Currently amended) The apparatus as claimed in claim [[13]] 27 ~~for use in a phase lock loop~~ having a reference signal and a loop feedback signal and wherein the reference signal is input to the clock input of the first storage element and the loop feedback signal is input to the clock input of the second storage element, and the provision of the stretching element for stretching the trailing edge of the output of one of the first and second storage elements enables the introduction of a compensatory phase offset at the input of the phase detection apparatus when the apparatus is used as a phase frequency detector in a phase lock loop.

27. (Currently amended) A phase lock loop apparatus having a reference signal input and an oscillator output, the apparatus comprising:

a) a filter element having an input and an output,

b) a controllable oscillator device having an input coupled to the output of the filter element and an output adapted to produce the oscillator output,

c) a frequency dividing element having a first input coupled to the output of the oscillator output and an output for producing a feedback loop signal,

d) a charge pump having two inputs and an output adapted to provide a phase difference signal as an input to the filter element, and

e) a phase detection apparatus comprising:

i) a first storage element having a clock input coupled to the reference signal input, a reset input and an output,

ii) a second storage element having a clock input coupled to the loop feedback signal, a reset input and an output,

iii) a logic element for logically combining the outputs of the first and second storage elements, the logic element having two inputs coupled to the outputs of the two storage elements and an output coupled to the reset input of the first storage element and the reset input of the second storage element, and

iv) a stretching element for effecting a stretching of the trailing edge of the output of one of the first and second storage elements relative to the other storage element, and wherein the outputs of the first and second storage elements are coupled to the inputs of the charge pump.

28. (Original) The phase lock loop apparatus as claimed in claim 27 wherein the frequency dividing element is coupled to an interpolator.

29. (Currently amended) The phase lock loop apparatus as claimed in claim 27 wherein the charge pump has a first input and a second input, the first and second inputs being coupled to the outputs of the first and second storage elements, respectively.